REMARKS

By this amendment, claim 36 is canceled, claims 34 and 53 are amended, and claims 54-59 are added for the Examiner's consideration. The above new claims do not add new matter to the application and are fully supported by the specification. For example, support for the amendment to claim 34 and new claims 54-59 can be found in paragraph [0039] of the instant published application No. 2006/0047474. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Allowed Claims

Applicants appreciate the indication that claims 19-23 and 44-46 contain allowable subject matter and would be allowed if presented in independent form. However, at this time, these dependent claims are not being presented in independent form because it is believed that the independent claims, from which they depend, are allowable. Moreover, Applicants submit that all claims are in condition for allowance for the following reasons.

35 U.S.C. §102(e) Rejection

Claims 1-18, 24-43 and 47-53 are rejected under 35 U.S.C. §102(e) as being anticipated by US Patent Application Publication No. 2004/0075140 to BALTES et al. This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the

subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation cannot be established because BALTES fails to teach each and every element of the claims.

In particular, independent claim 1 recites, *inter alia,*

> calculating a temperature of the first heating device using the measured change in the at least one electrical characteristic.

Additionally, independent claim 25 recites, *inter alia,*

> calibrating the measurement transistor by measuring a particular electrical characteristic of an active region of the measurement transistor with the measurement transistor held at a known temperature;
> incrementally measuring a change in the at least one electrical characteristic of the measurement transistor caused by the heat generated at the heating transistor; and
> calculating a temperature of the heating transistor using the measured change in the at least one electrical characteristic.

Furthermore, independent claim 34 recites, *inter alia,*

> the transistor configured to generate heat and the transistor configured to sense temperature being arranged on the silicon island; and
> a common source contact being arranged on the silicon island and leading to the source of both the transistor configured to generate heat and the transistor configured to sense temperature.

Still further, independent claim 39 recites, *inter alia,*

> at least one sensing field effect transistor arranged within the at least one silicon island corresponding to each heating field effect transistor of the at least one heating field effect transistor, wherein each sensing field effect transistor is arranged a prescribed distance from its corresponding heating field effect transistor and each sensing field effect transistor is configurable to sense a temperature.

Moreover, independent claim 47 recites, *inter alia,*

> three silicon sections;

three pairs of active regions, wherein each pair of active regions is arranged on a respective silicon section, wherein each pair of active regions is configurable to produce and sense heat; and
three thermal conductors, wherein each thermal conductor is arranged between each active region of each respective pair of active regions.

Finally, independent claim 53 recites, *inter alia*,

arrange a common source contact on a SiGe island, the common source contact leading to a source of both a first heating device and a first sensing device.

Applicants submit that BALTES does not disclose, or even suggest, at least these features.

Applicants acknowledge, for example, that BALTES discloses a device utilizing an Si island 12, a membrane 11, a poly-silicon resistor heater 13 arranged in the membrane 11, a plurality of temperature sensors 14 and 15 arranged at predetermined distances, and a plurality of contact electrodes 16 (see Fig. 3 and paragraphs [0074] – [[0079]). However, the Examiner has not identified any language in BALTES which discloses or suggests calculating a temperature of the first heating device using the measured change in the at least one electrical characteristic (claim 1). Applicants submit that BALTES instead (see paragraph [0083]) discloses that the various sensors 14.15 can measure "temperature distribution over the membrane" (emphasis added).

The Examiner has also failed to identify any language in BALTES which discloses or suggests calibrating the measurement transistor by measuring a particular electrical characteristic of an active region of the measurement transistor with the measurement transistor held at a known temperature, much less, incrementally measuring a change in the at least one electrical characteristic of the measurement transistor caused by the heat generated at the heating transistor, and calculating a temperature of the heating transistor using the measured change in the at least one

electrical characteristic (claim 25). Again, BALTES is apparently concerned with using the various sensors 14/15 to measure "temperature distribution over the membrane" (emphasis added) and not calculating a temperature of the heating transistor using the measured change.

The Examiner has also neglected to identify any language in BALTES which discloses or suggests a transistor configured to generate heat and a transistor configured to sense temperature being arranged on the silicon island, much less, a common source contact being arranged on the silicon island and leading to the source of both the transistor configured to generate heat and the transistor configured to sense temperature (claim 34). The device shown in Fig. 3 of BALTES instead merely discloses a poly-silicon resistor heater 13 and various contacts 16 arranged on the membrane 11.

The Examiner has also neglected to identify any language in BALTES which discloses or suggests at least one sensing field effect transistor arranged within the at least one silicon island corresponding to each heating field effect transistor of the at least one heating field effect transistor, wherein each sensing field effect transistor is arranged a prescribed distance from its corresponding heating field effect transistor and each sensing field effect transistor is configurable to sense a temperature (claim 39). Again, the device shown in Fig. 3 of BALTES instead merely discloses a poly-silicon resistor heater 13 and that the sensor 14 is arranged within the membrane 11 and not the Si island 12.

The Examiner has also failed to demonstrate that BALTES discloses or suggests three silicon sections, three pairs of active regions, wherein each pair of active regions

is arranged on a respective silicon section, wherein each pair of active regions is configurable to produce and sense heat, and three thermal conductors, wherein each thermal conductor is arranged between each active region of each respective pair of active regions (claim 47). Instead, the device shown in Fig. 3 of BALTES discloses one active region having a poly-silicon resistor heater 13, sensors 14/15, contacts 16, a membrane 11, and an Si island 12.

Finally, the Examiner has failed to demonstrate that BALTES discloses or suggests a common source contact arranged on a SiGe island, wherein the common source contact leads to a source of both a first heating device and a first sensing device (claim 53). The device shown in Fig. 3 of BALTES instead merely discloses a poly-silicon resistor heater 13, temperature sensors 14/15, and various contacts 16 arranged in the membrane 11 and not on the Si island 12, much less, an SiGe island.

Thus, Applicants respectfully submit that independent claims 1, 25, 34, 39, 47 and 53, and dependent claims 2-18, 24, 26-33, 35-38, 40-43 and 48-52 are allowable.

Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(e) should be withdrawn.

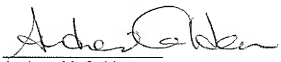
New Claims are also Allowable

Applicants submit that the new claims 54-59 are allowable over the applied art of record. Specifically, claims 54-59 depend from claims 1, 25, 34, 39, 47 and 53 which are believed to be allowable. Furthermore, claims 54-59 further recite a combination of features which are clearly not disclosed or suggested by the applied art of record. Accordingly, Applicants respectfully request consideration of these claims and further requests that the above-noted claims be indicated as being allowable.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to **IBM Deposit Account No. 09-0456** (Burlington).

Respectfully submitted,
Paul A. HYDE et al.



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